A Low-Power VLSI Neural Processor Design for High-Speed Image Data Compression in a SOI CMOS Technology

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Abstract

This paper presents a low-power VLSI neural processor that has been developed for high-speed vision processing based upon the frequency-sensitive self-organization (FSO) neural algorithm. Performance of this self-organization neural algorithm is proved to be efficient for adaptive vector quantization and can achieve near-optimal results. A system-on-chip design of the whole FSO neural system is described. Analysis of non-idea semiconductor effects on the FSO neural system chip design is presented. The prototyping chip for a 512-member competitive processor, which is a key functional unit of the FSO neural system, has been designed and fabricated in a 0.25-micron SOI CMOS technology via the MIT Lincoln Lab. It occupies a silicon area of 1.0 mm x 1.0 mm. It operates at 50 MHz and consumes about 10 mW. The competitive processor provides a computing capability as high as 25 giga-operations per second.

1. Introduction

The fundamental theory of self-organizing neural networks was presented by Grossberg [1], Kohonen [2], and other researchers [3, 4]. One major challenge of using a basic self-organization neural network is that some of the neural units may be under-utilized. The frequency-sensitive self-organization (FSO) method has been proposed to address this problem and proved to be effective to produce near-optimal results [5,6]. The frequency-sensitive self-organization method modifies Grossberg's variable-threshold competitive learning method by applying a winning frequency and its

associated upper-threshold value to the centroid-based learning rule. It systematically distributes the codevectors in the vector space R^n to approximate the unknown probability density function of the training vectors. Codevectors quantize the vector space and converge to cluster centroids.

The FSO method has been proved to be very efficient and can achieve near-optimal results for high-speed image compression and pattern recognition which adapting to the changing-source data statistics [5,6]. The popular LBG algorithm is difficult to implement for adaptive image compression and pattern recognition because it requires that the entire training data be processed in a batch mode [7].

In this paper, the frequency-sensitive self-organization neural network and its associated VLSI processor for high-speed vision processing applications is presented. Section 2 describes the self-organization neural network algorithm and data flow. Section 3 presents a massively paralleled VLSI neural processor to implement this algorithm. Section 4 discusses the non-idea effects on the neural network processor implementation. Section 5 presents the prototype chip and experimental results. The conclusion is given in Section 6.

2 The Frequency-Sensitive Self-Organizing Neural Network

The FSO neural algorithm is illustrated in Fig. 1 and described as follows:

Step 1: Initialize the codevectors $\mathbf{W}_i$ and the winning frequency F_i for each distortion-computing neuron:

$$\mathbf{W}_i(0) = \mathbf{R}(i), \qquad (1.1)$$
$$F_i(0) = 1,\ i = 1,\ ...,\ N,$$

where $\mathbf{R}(.)$ is a random vector-number generation function, M is the number of vector components, N is the number of codevectors, and $\mathbf{W}_i(0) = [W_{i1}(0),\ W_{i2}(0),\ ...,\ W_{iM}(0)]$. Notice that the first N input vectors can also be used as the initial codevectors instead of using results generated from $\mathbf{R}(.)$.

Step 2: Compute the distortion $D_i(t)$ between an input vector $\mathbf{X}(t)$ and all codevectors:

$$D_i(t) = d(\mathbf{X}(t),\ \mathbf{W}_i(t)) = \sum_{j=1}^{M} (X_j(t) - W_{ij}(t))^2, \qquad (1.2)$$

where t is the training vector index.

Step 3: Select the distortion-computing neuron with the smallest distortion and set its output $O_i(t)$ to high:

$$O_i(t) = \begin{cases} 1 & \text{if } D_i(t) < D_j(t),\ 1 \le i, j \le N,\ i \ne j, \\ 0 & \text{otherwise} \end{cases} \tag{1.3}$$

Step 4: Update the codevectors with a frequency-sensitive training rule and the associated winning frequency:

$$\mathbf{W}_i(t+1) = \mathbf{W}_i(t) + S(t)\, O_i(t)[\mathbf{X}(t) - \mathbf{W}_i(t)], \tag{1.4}$$

$$S(t) = \begin{cases} \dfrac{1}{F_i(t)} & \text{if } 1 \le F_i(t) \le F_{th}, \\ 0 & \text{otherwise,} \end{cases} \tag{1.5}$$

$$F_i(t+1) = F_i(t) + O_i(t), \tag{1.6}$$

where S(t) is the frequency-sensitive learning rate, and F_{th} is the upper-threshold frequency. Notice that only the winning codevector is updated. The training rule moves the winning codevector toward the training vector by a fractional amount which decreases as the winning frequency increases. If F_i is larger than F_{th}, then set S(t) to zero and no further training will be performed for this neural unit.

Step 5: Repeat Step 2 through Step 4 for all training vectors.

Use of the upper-threshold frequency can avoid codevector under-utilization during the training process for an inadequately chosen initial codebook. The selection of the upper-threshold frequency is heuristic and depends on source data statistics and training sequence. Empirically, an adequate F_{th} is chosen to be two to three times larger than the average winning frequency. The performance of the one-iteration FSO method can be incrementally improved by using iteration to adjust codevectors into better cluster centroids. The codebook obtained from the previous iteration is used as the initial values of the current iteration. After the first iteration, the upper-threshold frequency is not needed, because a good initial codebook is available. This method is called the multiple-iteration FSO method.

In the LBG method, the initial codebook could be obtained from the splitting-2 algorithm. The iteration of grouping and calculating centroids in the LBG method is similar to that of updating the closest codevector for each incoming data vector through the centroid technique in the FSO method. Therefore, the iterating FSO method without

the use of upper-threshold frequency asymptotically approximates the LBG method. If the learning process in the FSO method is repeated with the same termination criterion for the LBG method, the result of the multiple-iteration FSO method appears very close to that of the LBG method.

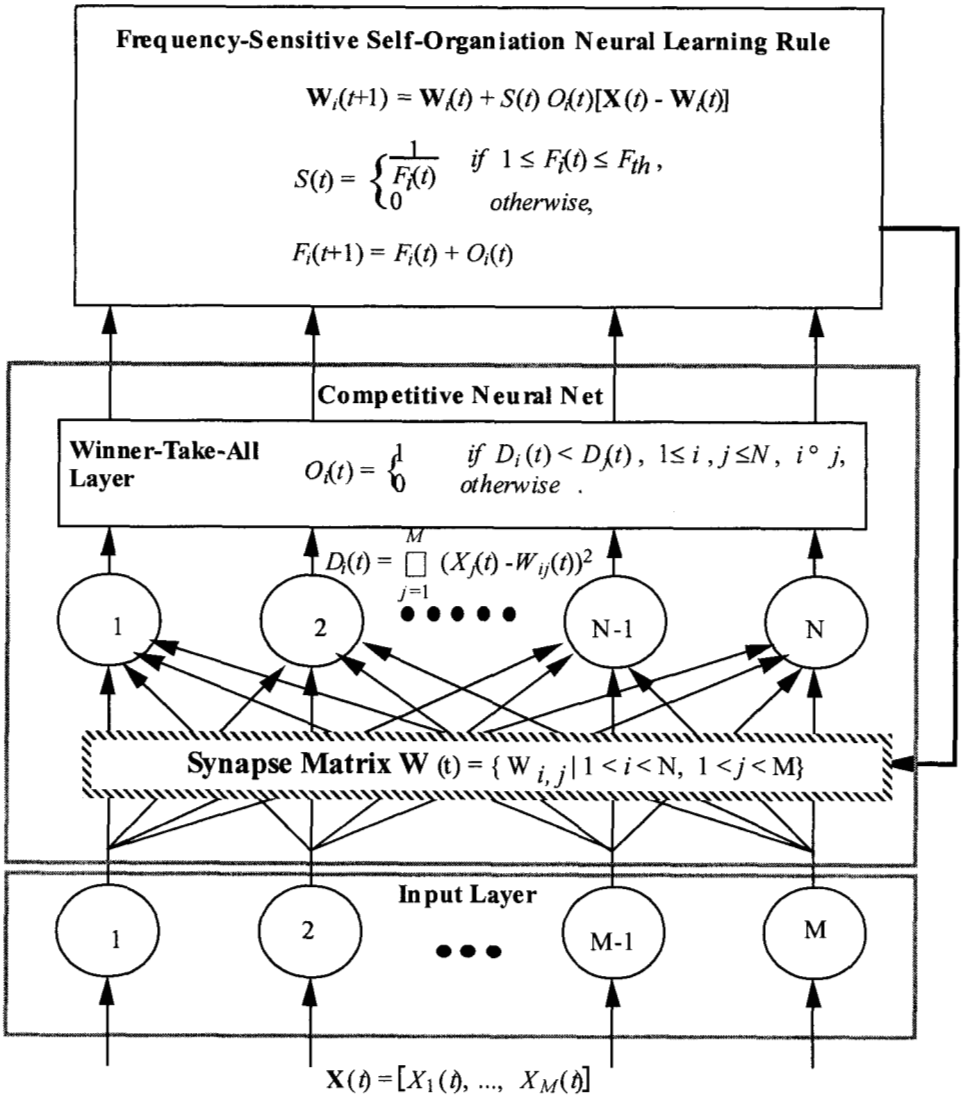


Figure 1: The frequency-sensitive self-organizing neural network.

3 A System-on-Chip Design of the Self-Organizing Neural Processor

A functional block diagram of the FSO neural system is shown in Fig. 2. By using the massively paralleled neural computing paradigm and the mixed-signal deep sub-micro technology, the whole neural computer can be implemented on a single VLSI chip. A system-on-chip (SOC) architecture design of the FSO neural system is shown in Fig. 3. This FSO neural chip can be an embedded neural computing engine to upgrade a general-purpose microcomputer into a supercomputing system for various high-speed intelligent information processing applications. A mixed-signal VLSI design technique is used for the FSO neural processor chip. The analog circuitry performs massively paralleled neural computation and digital circuitry processes multiple-bit address information.

The FSO neural processor chip realizes a full-search vector quantization process for each input vector at a time complexity *O(1)*. It consists of the input neurons, programmable synapses, summing neurons, winner-take-all cells, and an index encoder. The programmable synapse matrix is composed of M x N synapse cells, which correspond to N M-dimensional codevectors. The output neuron array is composed of N summing neurons, which perform paralleled summation of the distortions between the input vectors and codevectors. The winner-take-all block consists of N competitive circuit cells, which perform paralleled comparison among N *inverted* distortion values and choose a single winner. This block also provides a sufficiently high output level for the winning neuron against the rest. The index encoder circuit is an N-to-n decoder that uses binary codes to encode N classes.

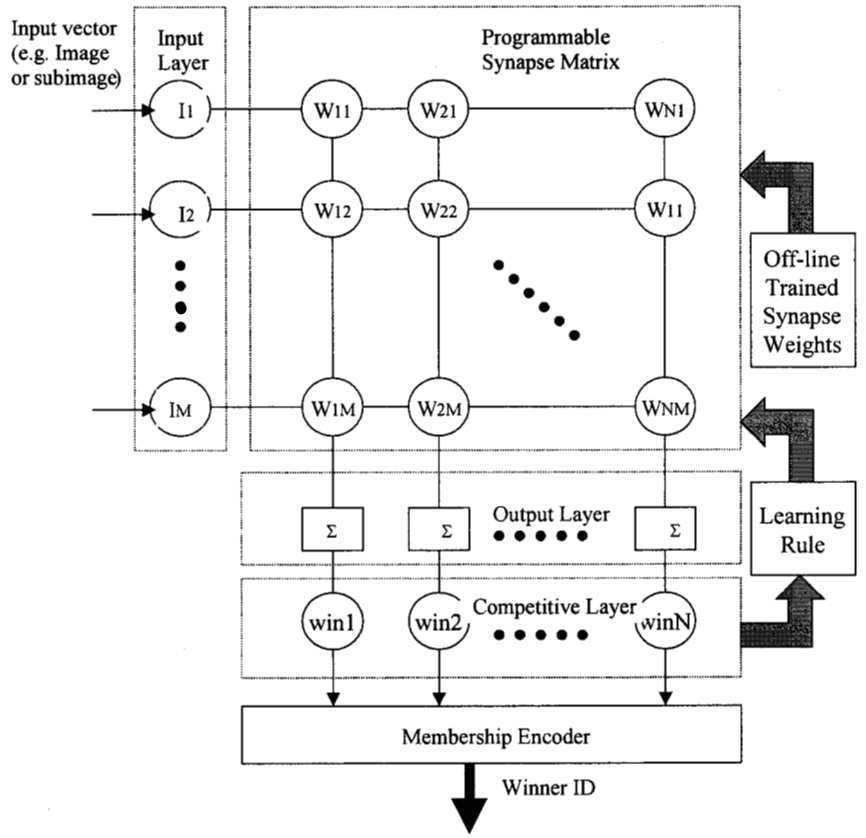


Fig. 2 A functional block diagram of the FSO neural network.

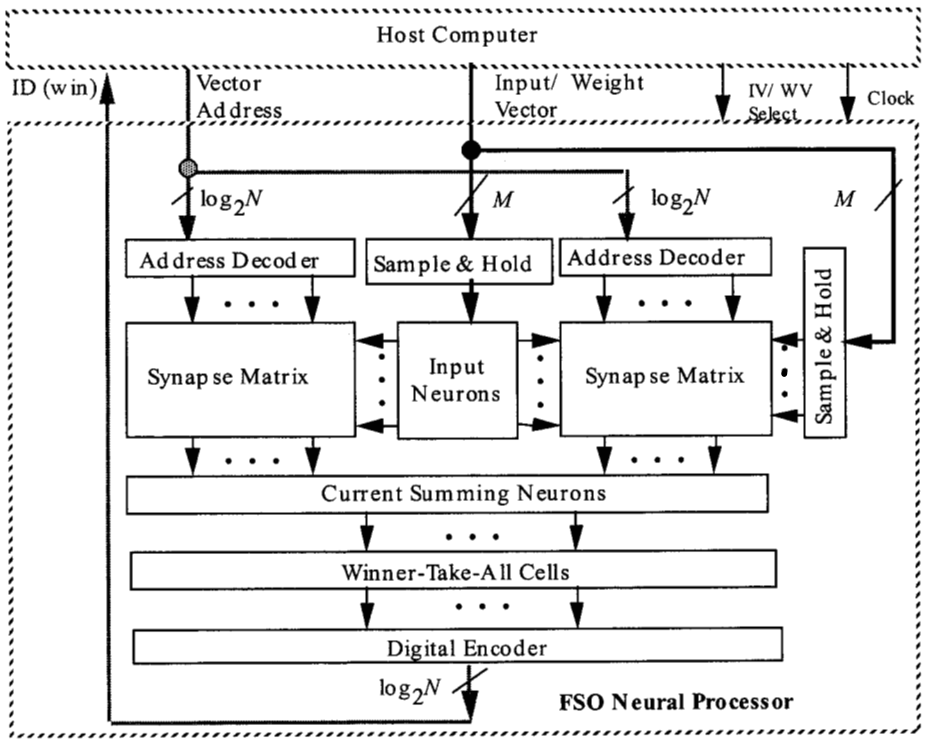


Fig. 3 A system-on-chip architecture design for the FSO neural system.

4. Analysis of Non-ideal Effects on the FSO Neural System

Fundamental limitations of analog neural computing are caused by non-ideal factors such as the process variation, transistor mismatches, and offset voltage. Several effects that determine the dimensionality of the network with the 8-bit accuracy are analyzed.

4.1. Effects of Device Variations on Neural Network Dimensionality

The operation of the network is restricted by the variations of device parameters such as process non-uniformity and transistor mismatches in synapse matrix. To consider the effect of the parameter variations of devices on the processing accuracy, two columns are considered among the synapse matrix. In two columns, all pairs of two synapse values are assumed to be the same except for one pair of synapse values as follows:

$$W_{1_i} = W_{2_i} = W_i \quad \textit{for all } i \textit{ and } i \neq k. \tag{4.1}$$

The summed output current in each column is expressed from Eq. (9) as

$$I_1 = I_{1k} + \sum_{i=1,\ i\neq k}^{M} I_{1_i}\,, \tag{4.2}$$

and

$$I_2 = I_{2k} + \sum_{i=1,\ i\neq k}^{M} I_{2_i}\,. \tag{4.3}$$

The difference of these two currents is

$$I_{out} \equiv I_1 - I_2 = I_{lsb} + I_{\Delta}\,, \tag{4.4}$$

where

$$I_{lsb} = \sqrt{\alpha_{1k}}(X_k - W_{1k})^2 - \sqrt{\alpha_{2k}}(X_k - W_{2k})^2, \tag{4.5}$$

and

$$I_{\Delta} = \sum_{i=1,\ i\neq k}^{M} (\sqrt{\alpha_{1_i}} - \sqrt{\alpha_{2_i}})(X_i - W_i)^2. \tag{4.6}$$

Here, I_{lsb} is the current determined from the desired synapse values, while I_{Δ} is the current due to the variations of the device parameters. Ideally, if there are no parameter variations in the devices, then I_{Δ} is zero and the difference current can be determined only from I_{lsb}. In practice, the absolute current value determined from the desired synapse values must be larger than that due to the device parameter variations. That is,

$$|I_{lsb}| > |I_{\Delta}|. \tag{4.7}$$

Considering the following conditions:

$$\alpha_{1k} = \alpha_{2k} = \alpha_0,\ \alpha_{1i} = \alpha_0(1 + \Delta),\ \alpha_{2i} = \alpha_0(1 - \Delta),$$

then Eqs. (4.5) and (4.6) become

$$|I_{lsb}| = |\sqrt{\alpha_0}\,[(X_k - W_{1k}) + (X_k - W_{2k})]\,(W_{1k} - W_{2k})| \tag{4.8}$$

and

$$|I_{\Delta}| = \left| \sum_{i=1,\ i\neq k}^{M} \sqrt{\alpha_0}\left(\sqrt{1+\Delta} - \sqrt{1-\Delta}\right)(X_i - W_i)^2 \right|, \tag{4.9}$$

respectively. For illustration purposes, assume that all inputs are to be matched to their weight values in the post-training process so that

$$X_i - W_i = V_m \text{ for all } i. \tag{4.10}$$

Then the number of the possible inputs is determined as

$$M < 1 + \frac{2|W_{1k} - W_{2k}|}{V_m\left(\sqrt{1+\Delta} - \sqrt{1-\Delta}\right)}. \tag{4.11}$$

In the case of 8-bit accuracy computation, the minimum difference of the synapse value is $V_{FS}/2^8$. V_{FS} is the full-scale dynamic range. The number of possible inputs in Eq. (4.11) is shown in Fig. 4 with respect to V_m. If the variation is within 1 %, then the 8x8 input can be applied with the matching between input and synapse values of 1% of the full dynamic range.

4.2. Effects of Parasitic Resistance on the Number of the WTA Cells

One of the main sources to restrict the number of the WTA cells to be connected side by side is the resistance along the common signal line. An analysis of the parasitic-resistance effects on the number of the WTA cells is given in this section.

Through the common signal line, the input currents are redistributed and compared one another. In general, the common signal line is made of the metal, of which sheet resistance is very small. However, the length of this line is so long that the resistance value cannot be ignored when the connected number of cells are large and comparison occurs between two far ends of this line. The voltage drop across the common signal line causes the gate-to-source voltage of each input transistor to be different although the applied input voltage is the same.

To analyze the effect of this finite resistance value along the common signal line on the number of the cells, simple model is introduced in Figure 4, where each cell is represented by the equivalent current source. The current flowing through each cell is I_B for the state of equilibrium. When an input voltage is applied to all cells, the current is represented by

$$I_j = I_B + \Delta_j \tag{4.12}$$

with the condition of

$$\sum_{j=1}^{N} \Delta_j = 0 \quad , \tag{4.13}$$

where N is the number of the competing cell. If the largest input voltage is applied to cell-1 as the winning input, then the difference of the input voltages between this cell and cell-i is expresses as,

$$V_{in}^1 - V_{in}^i = \sqrt{\frac{2}{\beta}} \left(\sqrt{I_B + \Delta_1} - \sqrt{I_B + \Delta_i}\right) + R \sum_{j=1}^{i} (i\text{-}j)\, \Delta_j \quad , \tag{4.14}$$

where $\beta = \mu C_{ox} (W/L)$ and R is the unit resistor value of the common signal line between two adjacent cells. The first term in (4.14) is the voltage difference for the different current assuming the perfect match of two cells. The second term in (4.14) is the voltage drop along the common line from cell-1 to cell-i, which is zero for the ideal case. Thus, for the proper WTA operation, the magnitude of the first term must be larger than that of the second term. In Fig. 5, the above two terms are shown for the two ends of cell-1 and cell-N given the following conditions:

$$I_1 = I_B + \left(\frac{N\text{-}1}{2}\right) \Delta \quad , \tag{4.15}$$

...

$$I_i = I_B + \left(\frac{N-1}{2} - (i-1)\right)\Delta, \tag{4.16}$$

...

$$I_{\frac{N+1}{2}} = I_B, \tag{4.17}$$

...

and

$$I_N = I_B - \left(\frac{N-1}{2}\right)\Delta, \tag{4.18}$$

where Δ is 80 nA. From the process parameter, the sheet resistance is known to be 0.026 Ω per square and there are 14 squares in the common signal line of each cell from the layout. About 600 cells can be connected in series as a row. Connecting raws in parallel can increase the number of the competing cells.

4.3 Analysis of Large Number of Winner-Take-All Cells

Let the inputs with the same input voltage level are assigned into groups 1 through L. The group i has n_i elements. The current flowing through each cell in group i is

$$I_i = \frac{\beta_1}{2}(V_i - V_{CM} - V_{th})^2. \tag{4.19}$$

The total bias current is distributed in the following way:

$$\sum_{i=1}^{L} n_i I_i = N I_B \tag{4.20}$$

and

$$N = \sum_{i=1}^{L} n_i \tag{4.21}$$

where N is the number of competitive inputs, and I_B is the bias current flowing in transistor M_5 of each cell. When the input voltage to the j-th group is the largest, the number of cells in the j-th group should be one and the current flowing in this cell, I_j, should be larger than the current flowing through a single cell in any other group to ensure the winner-take-all operation,

$$I_j > \max\{I_i,\ i = 1, 2, ...,\ L, \text{ and } i \neq j\} \tag{4.22}$$

or equivalently

$$V_j > \max \{V_i, i = 1, 2, ..., L, \text{ and } i \neq j\}. \quad (4.23)$$

To facilitate the analysis of this WTA circuit in a large network, the following conditions are assumed. There are three groups of input voltages: the winning voltage V_W, the second largest input voltage V_L, and the smallest one V_S. The numbers of cells in these groups are 1, L, and N-L-1, respectively. From Eq. (4.19), the current flowing through a single cell in each group can be expressed as

$$I_W = \frac{\beta_1}{2}(V_W - V_{CM} - V_{th})^2, \quad (4.24)$$

$$I_L = \frac{\beta_1}{2}(V_L - V_{CM} - V_{th})^2,$$

and

$$I_S = \frac{\beta_1}{2}(V_S - V_{CM} - V_{th})^2.$$

The total current is

$$I_{total} = 1 \times I_W + L \times I_L + (N-L-1) \times I_S. \quad (4.25)$$

In Fig. 6, calculated results for a 1000-input WTA circuit are shown. V_W, V_L, and V_S are set to 2.51, 2.50, and 2.49 V, respectively. As the number of the second largest input increases, the current flowing into the winning cell decreases monotonically. This results from the fact that more current is consumed by the cells in the second group, while the total bias current is constant. In Fig. 6(a), calculated results of the output levels are shown. In Fig. 6(b), the response time of the winning output voltage is shown. The output level of the winning cell decreased due to the reduced available current. Similarly, the response time of the circuit increased, because the amount of charging current was reduced.

In the case where the differences between competitive inputs are small, the performance of the WTA circuit can be degraded severely. The resultant input current in the winning cell is not large enough to be completely differentiated from all losing cells. Thus, the output voltage difference between the winning and losing cells is not large enough to be directly interfaced with the digital index encoder, because the winning cell output has intermediate value between 0 and 5 V. Although the winning output is still

larger than any other output, the response time for the above condition is quite long. More charging current is consumed by the transistor *M3* (Fig. 7), which is now biased in the linear region. To circumvent these problems, a cascaded version of the winner-take-all circuit can be used.

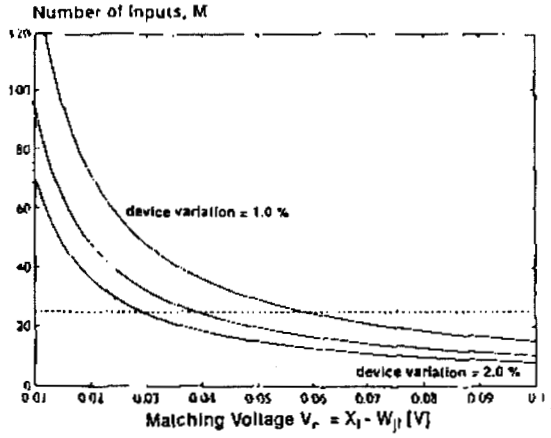


Fig. 4 The number of the possible dimensionality versus the matching voltage with different device variations.

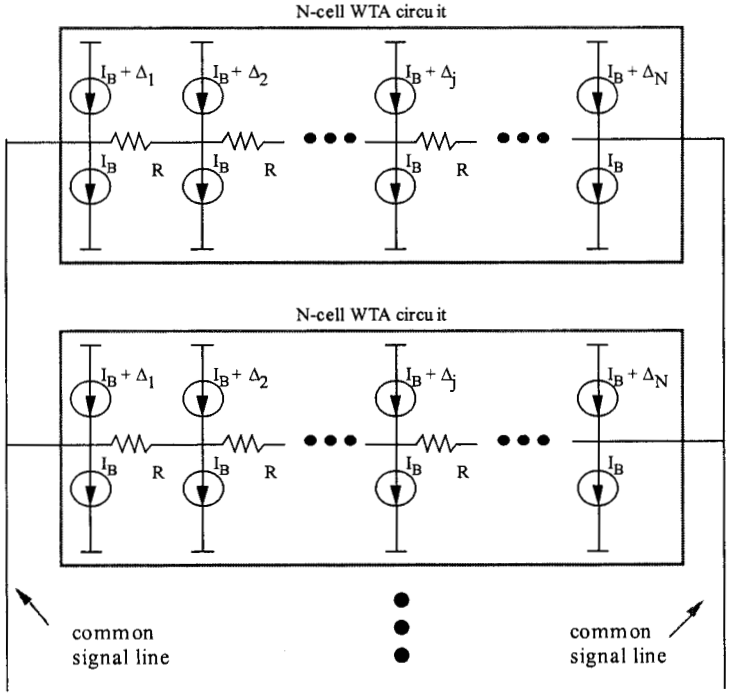
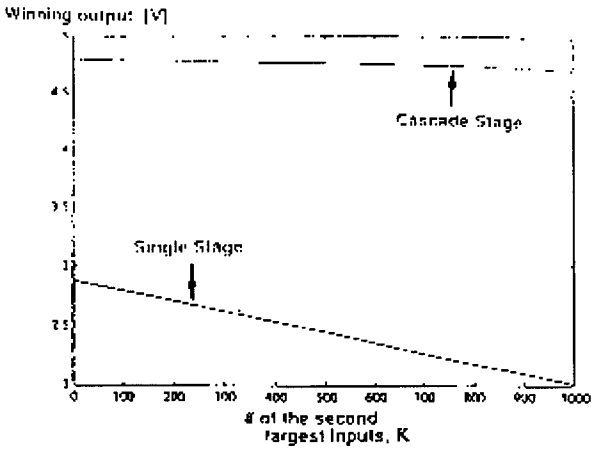
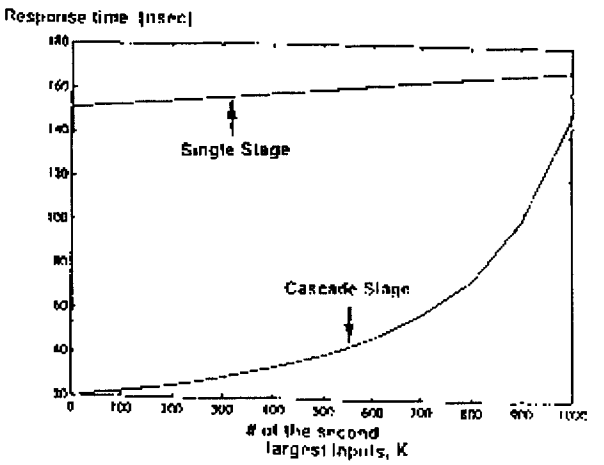


Fig. 5 Simple model of the winner-take-all circuit.





(a) (b)

Fig. 6 Calculation results on a 1000-input WTA with different numbers of cells having the second largest input voltage value.

(a) DC level of the winning output.

(b) Response time of the winning output.

5 VLSI Prototyping Chips for the FSO Neural System

5.1. A VLSI Prototype Chip for the FSO Neural System in a Scalable Bulk CMOS Technology

A VLSI prototype chip for the FSO neural processor was fabricated in a silicon area of 4.6 mm x 6.8 mm using the scalable bulk CMOS technology from the MOSIS Service of the USC/Information Sciences Institute at Marina del Rey, CA [5]. This prototype chip includes 25 input neurons, 25 x 64 synapse weight cells, 64 output summing neurons, 64 winner-take-all cells, and a 64-to-8 membership encoder. The die photo of this FSO neural chip is shown in Fig. 7. This chip can also be extended to implement a large-scale FSO neural system. An adaptive vector quantizer of 1024 codevectors can be implemented by cascading 16 such prototype chips or by using a larger design in a submicron fabrication technology.

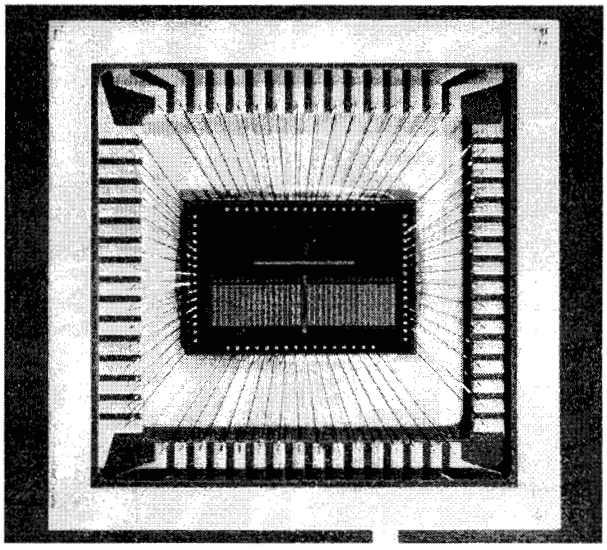


Fig. 7 A chip photo of the FSO neural system prototype chip in a scalable 2-micron bulk CMOS technology. The die size is 4.6 mm x 6.8 mm.

5.2. A VLSI Prototype Chip for the 512-member Winner-Take-All Competitive Processor of the FSO Neural System in a 0.25-micron SOI CMOS

Today's complex integrated circuits are fabricated almost exclusively in CMOS on standard silicon substrates. The availability of inexpensive, high-quality silicon wafers and rich manufacturing experience, favor standard CMOS for most applications. However, the migration toward smaller transistor dimensions, the need to decrease power dissipation, and a desire to combine sensitive analog circuits with complex digital circuits, has spurred interest in alternatives to standard CMOS technology, such as SOI.

With SOI technologies, circuits are fabricated in a very thin layer of silicon on an insulating substrate, or in a thin layer that is electrically insulated from a solid silicon substrate. Compared with bulk CMOS process, where the conductive silicon substrate contributes large parasitic capacitance, SOI technology is free from this major drawback. This provides the advantage of lower power consumption and higher operation speed. Furthermore, the reduced junction area and the absence of body effect provide the advantage of increased performance at low voltage. It has been proven in many circuits that SOI is a good candidate for low power, low voltage, and high performance applications. In order to exploit the low power and high-speed application, an SOI fabrication process has been selected. The fabrication technology chosen to implement the FSO neural processor is MIT/LL 0.25um low power SOI process. This is a fully depleted silicon-on-insulator CMOS process with single level poly, and triple level metal with stacked vias.

The existing 2-micron-bulk-CMOS FSO neural chip (4.6 mm x 6.8 mm) can be converted into a 0.25-micron-SOI-CMOS FSO neural chip at a size of 2 mm x 2mmm. Due to limitations of the allocated chip area (i.e. 1 mm x 1mm), the 512-winner-take-all competitive processor is therefore selected for the SOI-CMOS chip implementation. This 512- winner-take-all competitive processor is a major building block for the low-power large-scale FSO neural system.

5.2.1. Winner-Take-All Circuit Design and Simulation

A transistor-level diagram for the WTA circuit is shown in Figure 8. Each WTA cell consists of two identical cascaded stages (upper and lower stages). In each stage, the first portion (M_1, M_2, and M3) converts input voltage into the cell current, which is compared and redistributed along the common signal node, V_{cm1}. Each cell current, $I_{n,m1}$, is proportional to the square of the corresponding input voltage, $V_{in,n}^2$. The largest input voltage can therefore result in the largest amount of cell current. In the second portion (M_4, M_5), the cell current, $I_{n,m1}$, is mirrored to transistor M_4 and then converted into output voltage. If one of the input voltages, e.g. $V_{in,n}$, is sufficiently larger than other inputs, the output voltage, $V_{out,n}$, will saturate to the positive supply voltage while the rest will saturate at the negative rail. The binary output signals provide great advantages in interfacing with subsequent digital circuitry. The two-stage cascaded scheme provides better amplification and improves the WTA comparison resolution, also results in a higher speed operation.

The simulated result for a cascaded-WTA is shown in Figure 8. This circuit consists of two comparison cells, each with an estimated output load capacitance of 0.1 *pF*. At V_{dd} of 2 V and input (V_{in2}) frequency of 50 MHz (V_{in1} is held at a constant voltage), V_{out2} approaches positive rail as V_{in2} greater than V_{in1}, while V_{out2} goes to negative rail, as shown in the simulation result.

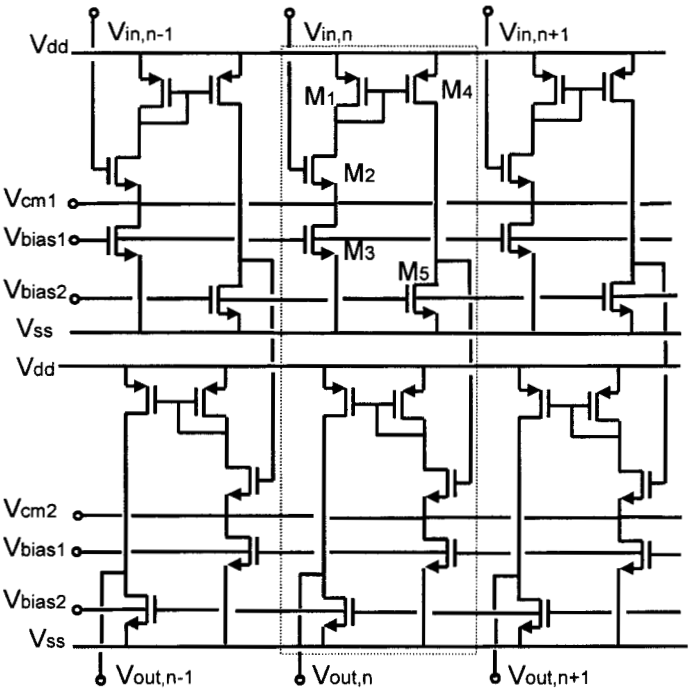
The performance of the WTA circuit built with transistors biased in the subthreshold region [8] is moderately limited due to the inherently low-speed operation and small noise immunity. Our modified WTA circuit operates in a strong inversion region and can provide fully binary output values that are easily interfaced with digital circuitry for network learning. Our analog WTA circuit can determine the winning cell at one cycle, instead of $\log_2 N$ clock cycles using MAXNET [9].

5.2.2. A Layout Design for the 512-Cell Winner-Take-All Competitive Processor

To fully test the 512-cell WTA circuit, it would require at least 512 input/output signals and other biasing supplies, which is not area-efficient in this chip implementation.

To reduce the required pad numbers, the whole WTA circuit is carefully grouped into 8 sections based on signal flow, cell position, capacitance loading effect, and I/O pads position. Therefore only 20 pins are needed for this prototype chip. Since only one WTA cell output will be 'high' in each comparison cycle and the rest will be 'low', an 8-to-3 encoder is implemented on-chip to further reduce the required output pin numbers.

Testing of VLSI neural network chips is an important task in constructing artificial neural systems. This winner-take-all competitive processor chip in the MIT 0.25-micron SOI CMOS has been designed and submitted in July 1998. Currently, this experimental chip is still in the fabrication process and to be delivered soon. Thus the experimental results will be reported after the chip is received and tested in near future.



Transistors (1st stage)	M1	M2	M3	M4	M5
Size: L/W (μm/μm)	1/0.25	0.5/0.25	0.5/0.25	1/0.25	0.5/0.25
Transistors (2nd stage)	M1	M2	M3	M4	M5
Size: L/W (μm/μm)	1/0.25	0.5/0.25	0.5/0.25	3.75/0.25	1/0.25

Figure 7. A transistor-level diagram for the Winner-Take-All circuit.

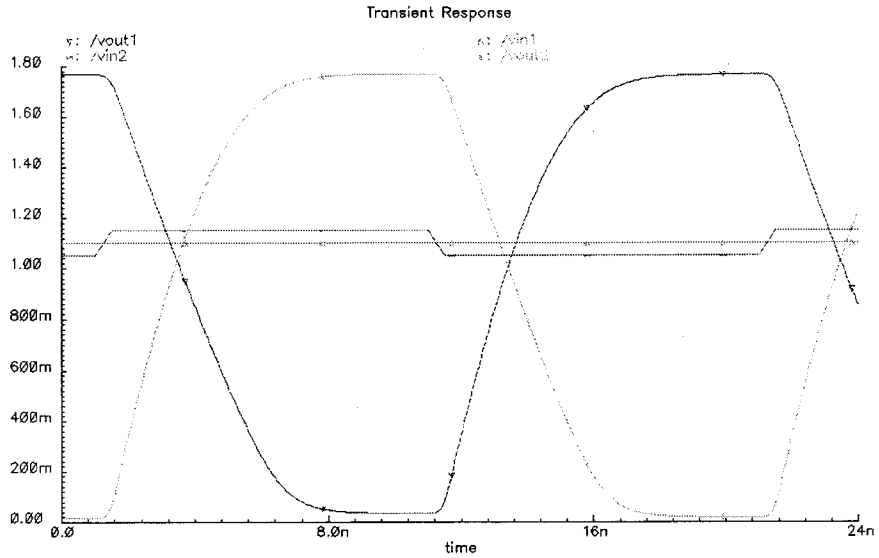


Figure 8. Simulation results of the modified WTA circuit.

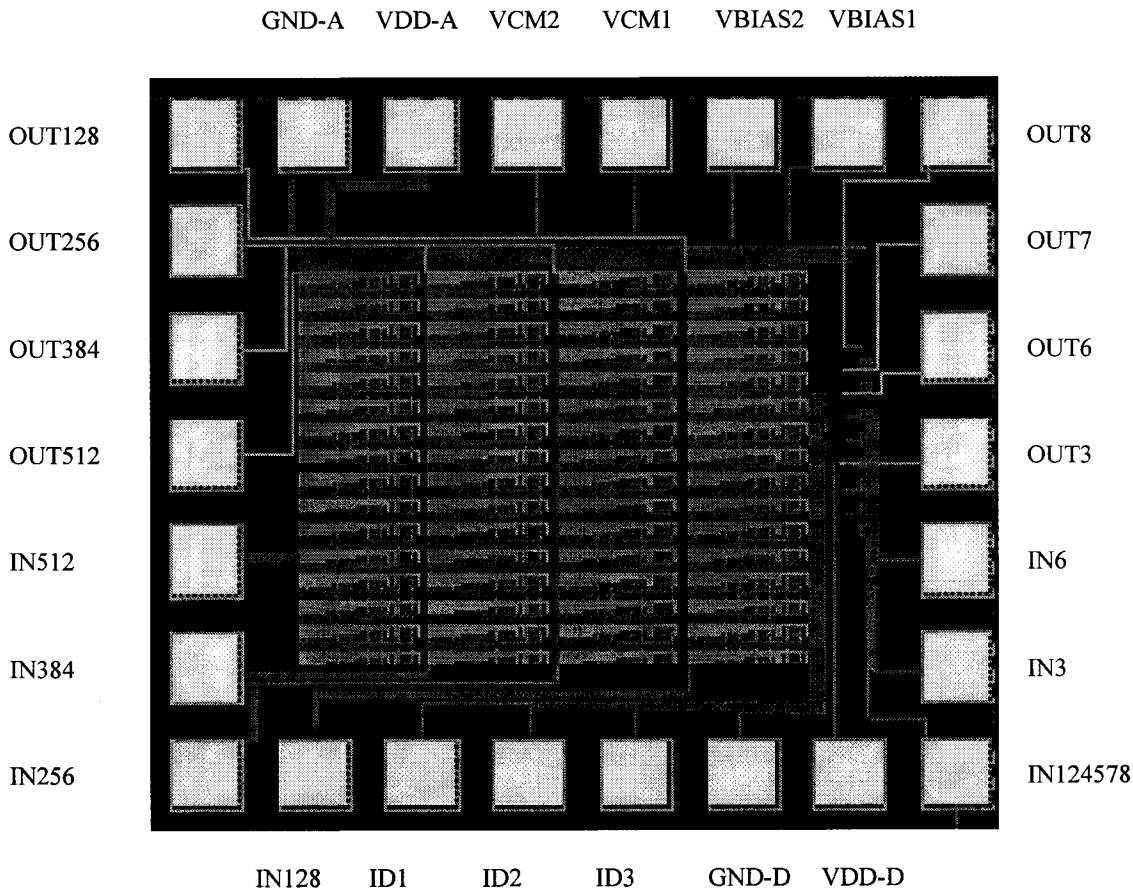


Figure 9. A chip layout design for the 512-member winner-take-all competitive neural processor in the MIT-LL 0.25-micron SOI CMOS technology.

6 Conclusion

The FSO algorithm and its associated system-on-chip design have been developed for high-speed image compression and pattern recognition which adapting to the changing-source data statistics. By using a mixed analog-digital design approach in the massively paralleled computation blocks, the advantages of small silicon area, low power consumption, and reduced I/O requirement can be achieved. The self-organization neural network algorithm and its data flow are described in details. The non-idea effects on the FSO neural network chip implementation is analyzed. The bulk-CMOS FSO neural chip was successfully designed, fabricated, and tested. This FSO neural chip has been under an upgrade study and can be easily converted into a SOI-CMOS chip at a smaller size and a much lower power. The 512-member competitive neural processor, which is one major building block of a large-scale FSO neural system, has been designed and fabricated in a MIT 0.25-micron SOI CMOS technology. Its estimated power dissipation is about 10 mW at a throughput rate of 50 MHz. Its equivalent computation power is about 25 giga-comparisons per second.

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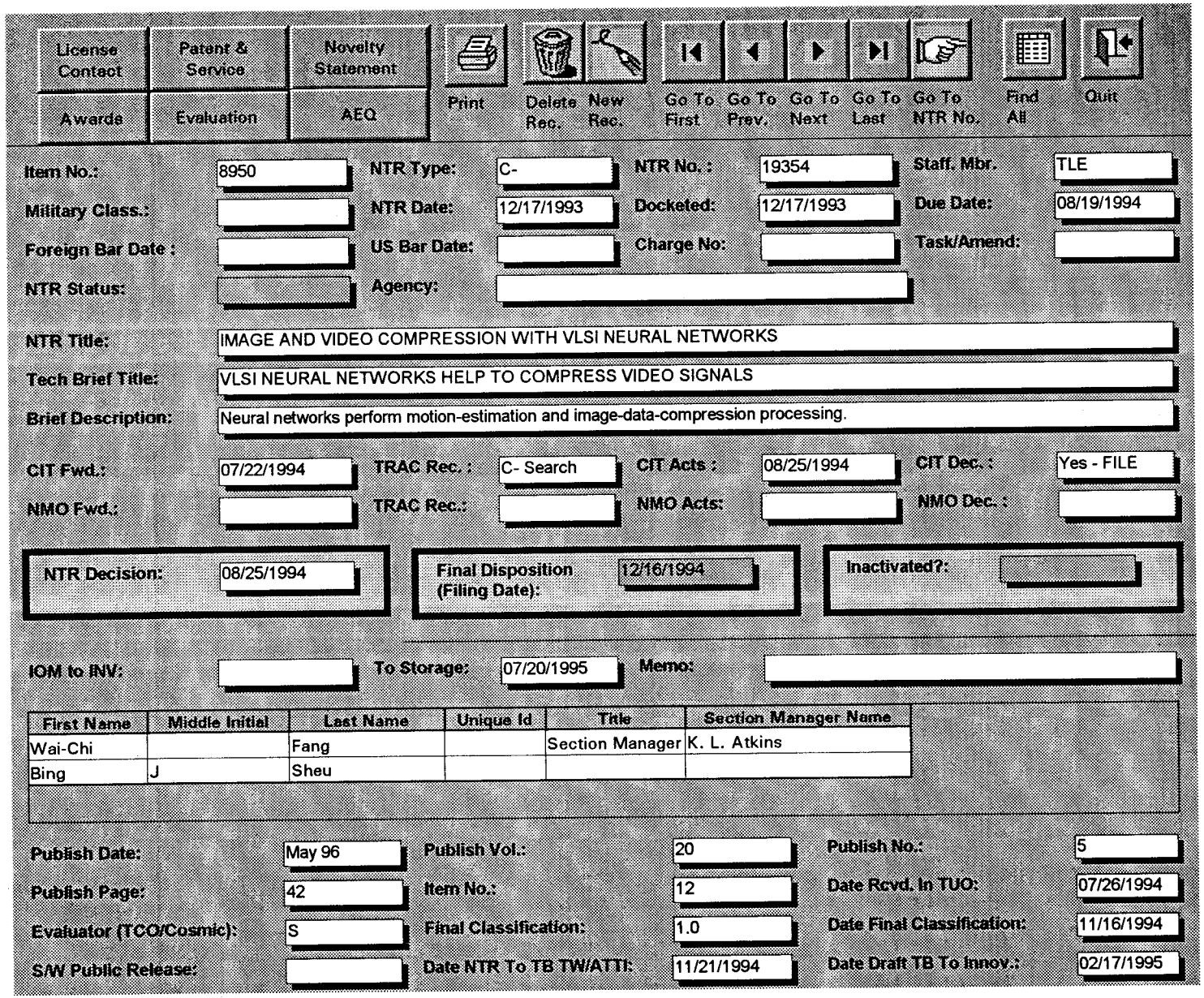
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